NON-VOLATILE MEMORY DEVICE AND FABRICATION METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 91105279, filed on March 20, 2002.

BACKGROUNDING OF THE INVENTION

Field of Invention

[0001] The present invention relates to a read-only memory device and the fabrication method thereof. More particularly, the present invention relates to a non-volatile read only memory device and the fabrication method thereof.

Description of Related Art

[0002] The current fabrication method for a non-volatile read only memory device comprises forming a trapping layer on a substrate, wherein the trapping layer is a stacked structure formed with a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer. A read only memory device that uses an ONO composite layer as the trapping layer is known as a nitride read only memory (NROM). A polysilicon gate is then formed on the ONO layer, followed by forming a source region and a drain region on both sides of the ONO layer in the substrate.

[0003] The plasma used in the fabrication of a NROM causes a charge build-up on metal. This phenomenon is known as the "antenna effect". When a transient charge imbalance occurs, charges are injected into the ONO layer inducing a programming effect,

leading to the problem of a high threshold voltage. In general, the threshold voltage varies in a wild range of 0.3 V to 0.9 V.

[0004] Conventionally, the method to prevent the programming problem resulted from the antenna effect is to form a diode in the substrate connecting electrically with the word line. As the transient charges reach a specific value, the device is discharged by the electric breakdown of the diode. However, when the voltage induced by the charges is less than the breakdown voltage of the diode, the charges may still be injected into the ONO layer to induce the programming effect. In addition, such a design lowers the input voltage of the device and decreases the rate of the writing operation.

SUMMARY OF THE INVENTION

[0005] The present invention provides a non-volatile read only memory and the fabrication method thereof, wherein the plasma induced damages on a memory device are prevented.

[0006] The present invention provides a non-volatile read only memory and the fabrication method thereof, wherein the transient charge imbalance is obviated to prevent electric charges to be injected into the ONO layer, inducing the programming effect.

[0007] The present invention provides a non-volatile read only memory and the fabrication method thereof, wherein a high threshold voltage is prevented.

[0008] The present invention provides a non-volatile read only memory and the fabrication method thereof in which the programming problem due to the antenna effect, leading to a lower input voltage and a decrease in the rate of the writing operation is resolved

[0009] Accordingly, the present invention provides a non-volatile read only memory, wherein a word line is formed over a substrate, and the word line includes a metal layer and a polysilicon line. A trapping layer is located between the word line and the substrate. Moreover, the non-volatile read only memory further comprises a polysilicon protection line formed over the substrate. The polysilicon protection line electrically connects the word line and the grounded doped region in the substrate, wherein the resistance of the polysilicon protection line is higher than that of the word line.

[0010] The present invention provides another fabrication method for a non-volatile read only memory, wherein a non-volatile read only memory cell is formed on a substrate. A polysilicon protection line is further formed on the substrate. The polysilicon protection line and the word line of the non-volatile read only memory cell are connected, wherein the resistance of the polysilicon protection line is higher than that of the word line. Thereafter, a grounded doped region is formed in the substrate, followed by forming a contact on the substrate such that the contact connects the grounded doped region and the polysilicon protection line. A metal interconnect is then formed on the substrate. Subsequent to fab-out, a high voltage is applied to burn out the polysilicon protection line.

[0011] The present invention further provides another fabrication method for a non-volatile read only memory device, wherein a substrate comprising an isolation region is provided. A trapping layer is then formed on the substrate. After this, a polysilicon layer and a silicide layer are sequentially formed on the substrate. The above layers are further patterned to form a word line for the non-volatile read only memory and a polysilicon line. The thickness of a portion of the polysilicon line is reduced to form a

polysilicon protection line above the isolation region. Thereafter, a dielectric layer is formed on the substrate to cover the above devices. A first contact and a second contact that connect the silicide layer and a doped region in the substrate are further formed in the dielectric layer. After the completion of the fabrication process, a high current is applied to burn out the polysilicon protection line.

[0012] The present invention provides a fabrication method for an electrically connected polysilicon protection line with the substrate to guide the charges built up in a fabrication process to the substrate. Damages induced to the ONO layer of the non-volatile memory device and the programming effect are thus prevented. Subsequent to fab-out, a high current is used to burn out the polysilicon protection line, allowing the memory device to operate normally. The transient imbalance charges are discharged through the substrate to prevent the problems encountered in a high threshold voltage due to the trapping of charges in the ONO layer.

[0013] Since the resistance of the polysilicon protection line is higher than that of the word line, the polysilicon protection line is burnt out by using a high current after the manufacturing process is completed. Therefore, the input voltage is prevented from being lower to slow down the rate of the writing operation during a normal operation of the memory device.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0016] Figures 1A to 1E illustrate a process flow of fabricating a non-volatile read only memory according to a first aspect of this invention in a cross-sectional view;

[0017] Figures 2A to 2B illustrate a process flow of forming a polysilicon line and a silicide word line during the fabrication a non-volatile read only memory according to a second aspect of this invention in a top view and in a cross-sectional view, respectively;

[0018] Figures 3A to 3B illustrate a process flow of forming a polysilicon protection layer during a fabrication of a non-volatile read only memory according to the second aspect of this invention in a top view and in a cross-sectional view, respectively; and

[0019] Figures 4A to 4B illustrate a process flow of forming an interconnect during a fabrication of a non-volatile read only memory according to the second aspect of this invention in a top view and in a cross-sectional view, respectively.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] The present invention provides a fabrication method for a non-volatile read only memory device that prevents the plasma-generated antenna effect during the fabrication of the non-volatile read only memory.

[0021] Figures 1A to 1E illustrate a process flow of fabricating the non-volatile read only memory according to a first aspect of this invention in a cross-sectional view.

[0022] As shown in Figure 1A, a non-volatile read only memory cell 102 is formed on a substrate 100. The non-volatile read only memory cell 102 includes a trapping layer 104 and a word line 106 thereon, wherein the trapping layer 104 includes a stacked structure of a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer. The word line 106 includes a polysilicon line 105a and a metal layer 105b, wherein the metal layer 105b includes tungsten silicide (WSi_x). The substrate 100 further comprises an isolation region 108 that separates the memory cell region and the peripheral circuit region. The isolation region 108, for example, a field oxide layer.

[0023] Continuing to Figure 1B, a polysilicon protection line 110 is formed on the substrate 100, wherein the polysilicon protection line 110 is connected with the word line 106 of the non-volatile memory cell 102. The resistance of the polysilicon protection line 110 is higher than that of the word line 106. In other words, the resistance of the polysilicon protection line 110 is higher than the resistance of the polysilicon line 105a of the word line 106. Moreover, the polysilicon protection line 110 is extended to the peripheral circuit region through the isolation region 108.

[0024] Thereafter, as shown in Figure 1C, a grounded doped region 112 is formed in the substrate 100 in the peripheral circuit region, wherein at least a portion of the polysilicon protection line 110 is formed above the grounded doped region 112.

[0025] Referring to Figure 1D, a dielectric layer 114 is formed on the substrate 100, and a contact 116 is formed in the dielectric layer 114, wherein the contact 116 is connected to the grounded doped region 112 and the polysilicon protection line 110.

[0026] After this, as shown in Figure 1E, a metal interconnect 118 is formed on the substrate 100. A high current is then applied to burn out the polysilicon protection line 110 after the completion of the fabrication process, and the burnt out region 120 isolate the memory cell region and the peripheral circuit region. As a result, during the operation of the memory device, the input voltage is prevented from being lowered to reduce the rate of the writing operation by the polysilicon protection line 110.

[0027] The present invention provides a second aspect of fabricating another type of non-volatile read only memory, as shown in Figures 2A, 2B, 3A, 3B, 4A and 4B.

[0028] As shown in Figures 2A and 2B, a substrate 200 that comprises a field oxide layer as an isolation region 202 is provided. A trapping layer 204 is then formed on the substrate 200, wherein the trapping layer 204 includes a stacked structure of a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer. After this, a polysilicon layer and a silicide layer are sequentially formed on the substrate 200, followed by patterning the above layers to form the word line 208 of the non-volatile read only memory and the underlying polysilicon line 206, wherein the width of the patterned polysilicon line 206 and word line 208 above the isolation region 202 is smaller than that above other region. The word line 208 includes tungsten silicide (WSi_x).

[0029] Referring to Figures 3A and 3B, a patterned photoresist layer 210 is then formed on the substrate 200, wherein a portion of the word line 208 located above the isolation region 202 is exposed. After this, using the photoresist layer 210 as etching mask, the exposed word line 208 is removed. The etching is continued to the polysilicon line 206 underneath the word line 208 to reduce the thickness of the portion of the

polysilicon line 206 that is above the isolation region 202 to form a polysilicon protection line 206a at the region 212.

[0030] Continuing to Figures 4A and 4B, the photoresist layer 210 is removed followed by forming a doped region 214 in the substrate 200. A dielectric layer 216 is then formed on the substrate 200 to cover the above various devices. Contact 218a and contact 218b that respectively connect to the word line 208 and the doped region 214 in the substrate 200 are then formed in the dielectric layer 216 followed by an interconnect manufacturing process. The interconnect manufacturing process is, for example, forming a metal interconnect 220 on the dielectric layer 216 and the metal interconnect 220 connects with the contact 218a. Subsequent to fabrication process, a high current is then applied to burn out the polysilicon protection line 206a. Normally the burnt out region is the narrowest portion 212 of the polysilicon protection line 206a.

[0031] In accordance to the present invention, a polysilicon protection line that is electrically connected to the substrate is used to reduce the generation of charges, even under a high pressure environment of a plasma involved process. The transient imbalance charges can be discharged to the substrate through the polysilicon protection line to prevent damages induced on the ONO composite layer of the nonvolatile memory device or to prevent the programming effect, leading to a high threshold voltage.

[0032] Accordingly, damages induced on the trapping layer or inducing the programming effect are prevented through the polysilicon protection line. Moreover, a high current is used to burn out the polysilicon protection line subsequent to the manufacturing process to allow a normal function of the memory device.

[0033] Since the resistance of the polysilicon protection line of the present invention is higher than that of the word line, a high current is used to burn out the

polysilicon protection line subsequent to fab-out. Consequently, a lowering of the input voltage, leading to a decrease of the rate of the writing operation by the polysilicon protection line of the present invention is prevented.

[0034] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.